REMARKS

The Office Action dated May 28, 2008, addresses claims 1-4, 6-8 and 12-20. Claims 1-4, 6-8 and claims 13-20 are finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Penn et al. (U.S. Patent No. 6,731,976, "Penn") in view of Zierhofer (U.S. Patent No. 6,600,955, "Zierhofer") and further in view of "Najafi"[1]. Applicants gratefully acknowledge the Examiner's indication that claim 12 contains allowable subject matter.

By this response, Applicants amend claims 1 and 4 to correct obvious typographical errors, and claim 6 is amended to conform to the terminology of independent claim 1. No new subject matter is added by this amendment.

Applicants respectfully traverse the rejection of claims 1-4, 6-8 and 12-20. The Examiner asserts that the Penn patent teaches each and every element of independent claim 1, except "a sigma-delta (Σ-Δ) analog-to-digital converter to convert said analog bioelectric signal into a 1-bit data stream", which according to the Examiner is taught by Zeirhofer and Najafi. For all of the following reason, Applicants respectfully disagree with the Examiner and request reconsideration and withdrawal of the rejections.

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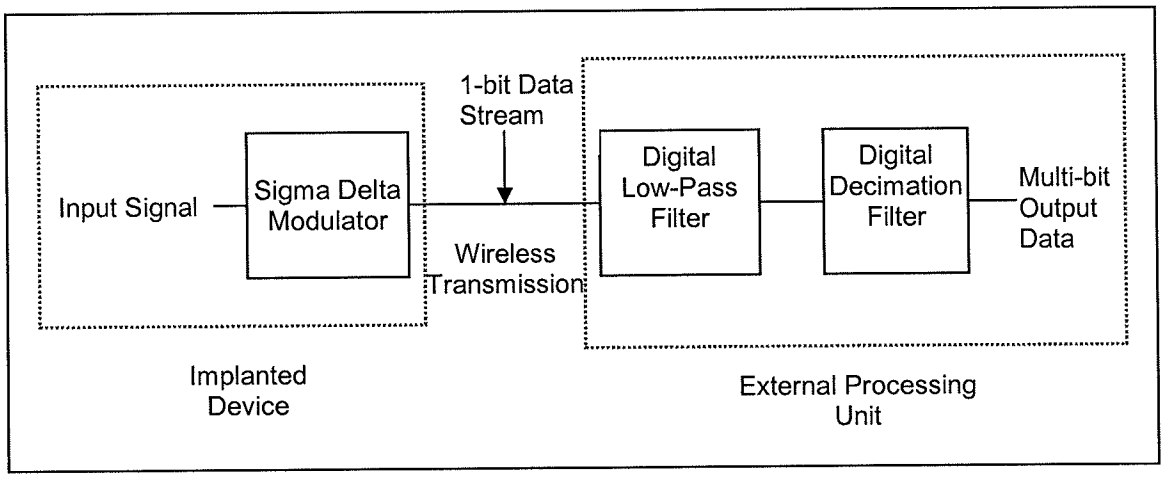
[1] The Examiner has failed to identify the Najafi patent in the Office Action. Based on the references made to the Najafi patent in the Office Action, Applicants assume that the Examiner is referring to U.S. Patent No. 4,211,048 to Najafi et al., which will be used for arguments by the Applicants hereinafter.

Claim 1 recites the following (emphasis added):

> 1. (Currently Amended) An implantable bioelectric signal processing system comprising:
>
> an interface configured to receive an analog bioelectric signal from at least one electrode implanted in said living organism;
>
> **a sigma-delta (Σ-Δ) analog-to-digital converter to convert [[the]] said analog bioelectric signal into a 1-bit data stream**;
>
> a transceiver coupled to said Σ-Δ analog-to-digital converter, said transceiver configured **to communicate said 1-bit data stream to a remote processing system over a wireless communications link**;
>
> wherein said 1-bit data is representative of the received analog bioelectric signal, which is further **filtered and processed in an external processor** to extract information about the received signal;
>
> an antenna coupled to a capacitor circuit, for receiving and storing power which is transmitted wirelessly from an external source, said capacitor circuit and antenna configured to indirectly stimulate the process of signal reception from said at least one electrode in response to [[the]] said transmitted power.

Claim 1 clearly recites that the implantable bioelectric signal processing system of the present disclosure includes a sigma-delta converter that converts the analog signal to a 1-bit data stream, which is then transmitted over a wireless communication link to a remote processing unit. The 1-bit data stream is filtered and processed in the remote processing unit to generate a multi-bit output data. The block diagram of a sigma-delta (Σ-Δ) analog-to-digital converter, as implemented in the present invention, is reproduced below to further clarify the components included

in the implantable logic circuit 10. One of ordinary skill in the art will understand that paragraph [0025] of the present disclosure fully supports this illustration. A detailed description of the principle of Σ-Δ modulation for analog-to-digital conversion is provided in Section 6 of the "Motorola Digital Signal Processors" handbook, which is attached herewith.



More specifically, a Σ-Δ converter is a combination of a sigma-delta modulator for converting the input signal into a 1-bit data stream, a digital low-pass filter which removes quantization noise, followed by a decimation filter which reduces the sampling rate down to the Nyquist rate to minimize the amount of information for subsequent storage, or digital signal processing. In the present disclosure, only the sigma-delta modulator part of the entire sigma-delta converter is included in the implanted logic circuit 10. The 1-bit data stream generated by the delta-sigma modulator is transmitted wirelessly to a remote processing unit where the digital filter section removes noise, reduces the sampling rate, and generates a multi-bit data

representative of the input signal. This is clearly depicted in FIG. 3 of the present disclosure, and further described in paragraph [0025].

> [0025] As shown in FIG. 3, the signal sampling carried by the sampling circuit 18 out on the implantable logic circuit 10 requires that an original analog signal 30 received through the implantable logic circuit input interface 12 be amplified at circuit 14 and converted to a digital signal 32 in the A/D digital converter circuit 16. Next, **using 1-bit sigma-delta (Σ-Δ) sampling, the digital signal is converted into a 1-bit data stream** 34 by the sampling circuit 18, wherein a "1" or high signal indicates an increase in signal amplitude, and a "0" or low signal indicates a decrease in signal amplitude. The resulting **1-bit data stream 34 is communicated via the wireless communications link 22 to the external signal processor 100, where it is filtered and processed as required,** depending upon the particular type of brain activity signal. Processing is preferably performed in the external signal processor 100 to **maintain the power consumption of the implantable logic circuit 10 at a reduced level** which can be adequately supplied via the wireless link.

(Causevic, paragraph [0025], emphasis added)

As further described in paragraph [0025], this particular arrangement reduces the power consumption of the implantable logic circuit 10, as the digital filter section consumes more power compared to the delta-sigma modulator.

Neither Zierhofer nor Najafi teaches or suggests this particular arrangement of a Σ-Δ converter, where only the front-end of the converter is placed in the implantable device, and the generated 1-bit data sequence is wirelessly transmitted to an external processing unit where the data is filtered for complete implementation of the sigma-delta ADC process. Furthermore, Zierhofer teaches that the data sequence generated by the sigma-delta modulator be stored to a memory in the implant before transferring the data to the outside via load modulation. See col. 6, ll.

50-55, and FIGS. 10(a) and 10(b). In the present disclosure, the 1-bit data stream is transmitted directly to the external processing unit without being stored in the implanted device.

Najafi, on the other hand, simply suggests sigma-delta analog-to-digital conversion as a possible conditioning circuit for implant 201. As shown in FIG. 3, and further described in col. 4, ll. 10-12 of Najafi, signal conditioning circuitry 211 is wholly integrated with electronic circuit 205 of implant 201. Najafi does not teach or suggest the splitting of the sigma-delta circuit, and transmitting only the 1-bit data stream from the sigma-delta modulator to a remote unit for filtering and processing of the 1-bit data sequence.

Therefore, neither Zierhofer nor Najafi teach all of the deficiencies in Penn that are required to satisfy each and every limitation of independent claim 1. Applicants respectfully requests that the rejection of claim 1 be withdrawn. Claims 2-4 and 6-8 depend from claim 1, and therefore, are allowable for at least the same reasons as claim 1.

As acknowledged by the Examiner, claims 13-20 are directed to a method for acquiring bio-electric signals from an organism, which is not distinct from the subject matter of claims 1-4 and 6-8 directed to an implantable bioelectric signal processing system. Therefore, claims 13-20 are allowable for at least the same reasons as claim 1.

It is respectfully submitted that the remarks presented here clarify the claims for the purposes of appeal, entry of which is earnestly solicited.

Conclusion

In view of the foregoing remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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By: _____

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